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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/944,263	08/30/2001	Sankaran M. Menon	42390P12429	1021

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EXAMINER

KERVEROS, JAMES C

ART UNIT	PAPER NUMBER
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2133

DATE MAILED: 12/15/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

09/944,263

Applicant(s)

MENON ET AL.

Examiner

JAMES C KERVEROS

Art Unit

2133

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 09 August 2004.  
2a) ☒ This action is FINAL. 2b) ☐ This action is non-final.  
3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 8-20 is/are pending in the application.  
4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.  
5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.  
6) ☒ Claim(s) 8-20 is/are rejected.  
7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.  
8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.  
10) ☒ The drawing(s) filed on 09 August 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).  
11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) ☐ All b) ☐ Some \* c) ☐ None of:  
1. ☐ Certified copies of the priority documents have been received.  
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

### **DETAILED ACTION**

1. This is a Non-Final Office Action in response to Amendment filed August 9, 2004, in reply to the Office Action, dated May 17, 2004.

Claims 1-7 are cancelled. Claims 8-20 are pending and are presently under examination.

2. Objection to the drawings is withdrawn in view of formal drawings submitted to the draftsman in a separate letter on August 9, 2004.

Objection to the specification is withdrawn in view of amendment to the Abstract

### ***Claim Rejections - 35 USC § 102***

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 8-20 are rejected under 35 U.S.C. 102(e) as being anticipated by

Adusumilli et al. (US 6334198), application filed: April 1, 1999.

Regarding independent Claims 8 and 14, Adusumilli discloses a method and a system comprising:

A plurality of cores, FIG. 1 showing an IC with multiple "core" circuits, such as multiple CPUs, with each core circuit including its own TAP controller, a first multiplexer (18) coupled to a first test access port controller TAP1 (12) and to a corresponding CPU core. A second multiplexer (20) coupled to a second test access port controller TAP2 (14) and to a corresponding CPU core. A first and a second pin, such as separate IC pins for selecting one of the TAP controllers for testing and/or debugging the IC, using the select signal of the first and second multiplexer MUX 18 and 20, respectively. The first pin controls the first select signal from TLM module to MUX 18 and the second pin controls the second select signal from TLM module to MUX 20, (see abstract and col. 1, lines 45-50).

Regarding Claims 9 and 15, Adusumilli discloses a plurality of Joint Test Action Group (JTAG) signals (TDI, TDO, TMS and TCK) which are fed TLM 16, and is used to control corresponding signals internally generated for coordination between the TLM 16 and the TAP controllers 12 and 14. These signals, such as (TDI, TDI1, TDO2) and second (TDI, TDI2, TDO1) are coupled to MUX 18 and 20, which include control and status signals, and select signals for routing data through the multiplexers (col. 4, lines 53-67).

Regarding Claims 10-12, 16 and 17, Adusumilli discloses a first pin corresponding to the select signal of MUX 18, which selects a core (CPU) and a second pin corresponding to the select signal of MUX 20, which selects either one of a functional mode of operation, or a debug mode of operation, or an emulation mode of operation, in response to a test mode select (TMS), which generates select signals for

routing data through (MUX 18 and 20). Typically, separate IC pins are used to select one of the TAP controllers for testing and/or debugging the IC.

Regarding Claims 13 and 18, Adusumilli discloses a second multiplexer MUX 20, which forwards the plurality of JTAG signals (TDI, TDI2, TDO1) to the second test access port controller TAP2 (14) for either a debug mode of operation or an emulation mode of operation, in response to TMS signal (test mode select).

Regarding Claim 19, Adusumilli discloses a first multiplexer MUX 18, which forwards the plurality of JTAG signals (TDI, TDI1, TDO2) to the first test access port controller TAP1 (12) for either a debug mode of operation, or an emulation mode of operation, or to test one of the cores (CPU), in response to TMS signal (test mode select).

Regarding Claim 20, Adusumilli discloses a second multiplexer MUX 20, which does not forward the plurality of JTAG signals to the second test access port controller, when the TMS is not in the test mode of operation, and the plurality of IC pins coupled to the second multiplexer MUX 20 are utilized for other functional purposes, such as normal mode of operation.

### ***Response to Arguments***

5. Applicant's arguments filed August 9, 2004 have been fully considered but they are not persuasive. Claims 8-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Adusumilli et al. (US 6334198), as set forth in the present Office Action.

In Reference to claims rejected under 35 U.S.C. 102(e) as being anticipated by Adusumilli, the Applicant argues that Adusumilli does not teach the claimed limitation of "selecting either a first test access port controller or second access port controller for a first mode of operation", recited in the independent claims 8 and 14. The Applicant further argues that Adusumilli alleviates the need to transfer control from one TAP controller to another.

In response to Applicant' argument above, clearly Adusumilli discloses a first multiplexer (18) coupled to a first test access port controller TAP1 (12) and a second multiplexer (20) coupled to a second test access port controller TAP2 (14), using the select signal of the first and second multiplexer MUX 18 and 20, respectively, for selecting one of the TAP controllers for testing and/or debugging the IC, Figure 1, in accordance with a first mode of operation", such as a TAG interface signal TMS (test mode select), which is fed to and received by the TLM 16, and is used to control corresponding signals internally generated for coordination between the TLM 16 and the TAP controllers 12 and 14. These signals include control and status signals, and select signals for routing data through the multiplexers 18 and 20 and also through output multiplexer 22.

***Conclusion***

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to JAMES C KERVEROS whose telephone number is (571) 272-3824. The examiner can normally be reached on 9:00 AM TO 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only.

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For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

U.S. PATENT OFFICE  
Examiner's Fax: (703) 746-4461  
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Date: 10 December 2004  
Office Action: Final Rejection

By: 

JAMES C KERVEROS  
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